

# LNA AND RF VGA FOR BROADBAND AND WIDE DYNAMIC RANGE DVB-S2 RECEIVER TUNER IN 0.18 $\mu$ M CMOS PROCESS

***Bhanu Shrestha & Nam-Young Kim***

Department of Electronic Engineering,  
Kwangwoon University,  
Seoul, S. Korea  
bnu@kw.ac.kr, nykim@kw.ac.kr

## ABSTRACT

We present a design of broadband and wide dynamic range low noise amplifier/radio frequency variable gain amplifier (LNA/RF VGA) for digital video broadcasting – satellite (DVB-S2) receiver tuner integrated circuit fabricated using the 0.18  $\mu$ m complementary metal oxide semiconductor (CMOS) process. The MOS switching filter was used to get broadband characteristics of the LNA circuit and the MOS channel resistance with two attenuators was used to obtain a wide dynamic range characteristic of the RF VGA. The LNA/RF VGA block achieved a gain control range of 50 dB, IIP3 of +15 dBm at low gain mode and a noise figure of 6.3 dB at the frequency range of 950 MHz ~ 2150 MHz. The RF VGA circuit consumed a total current of 28 mA with the supply voltage of 1.8 V and the chip area was 1.4 mm  $\times$  0.6 mm including I/O pads.

**Keywords:** LNA, RF VGA, DVB-S2, CMOS LNA, RF VGA.

## 1. Introduction

The digital video broadcasting – satellite (DVB-S2) is the latest advanced technique for the satellite transmission system that improves on and expands the range of capable applications. Therefore, it is also known as the second-generation specification for satellite broad-band applications that combine DVB-Satellite (DVB-S) and DVB, which was developed by the DVB project in 2003 [1]. It mainly offers the television applications including broadcasting, contribution TV links and digital satellite news gathering (DSNG). In DVB, there is revision from the existing DVB-S 1 to DVB-S2 for offering a much higher transmission capacity than the previous ones in the given repeater bandwidth and signal power. The purposes of standard revision are to guarantee a much higher transmission capacity and to improve service capability through the enhanced link margin and the realization of a new service requirement for broadband broadcasting like HDTV, interactive services, including internet access, digital TV contribution and news gathering, etc. There is a limitation with bandwidth

problems in the DVB-S1 system as Ka-band satellite broadcasting, and the carrier-to-noise (C/N) ratio has also been estimated to be about 0.5 dB/s during heavy rain fades in the first version of DVB-S [2, 3].

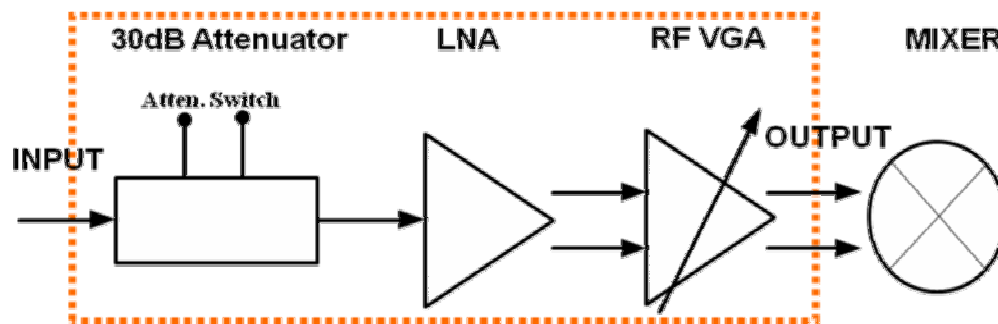


Figure 1. Block diagram of RF/VGA.

For this DVB-S2 tuner, the low noise amplifier/radio frequency variable gain amplifiers (LNA/RF VGA) are designed and fabricated using complementary metal oxide semiconductor (CMOS) technology which is the dominant integrated-circuit manufacturing technology. The block diagram of RF/VGA is shown in Figure 1. MOSFETs are the most widely used devices in modern integrated circuits. It can be predicted that CMOS will remain as a mainstream for foreseeable future technologies, and the reduction of CMOS device dimensions will continue. It is realistic to expect device performance to be increased, as efforts continue in technology scaling for the next decade; however, fundamental materials and processing changes is essential [4].

## 2. Circuit Design Techniques

### 2-1. MOS Attenuator

In order to control signal levels in the receiver, adjustable attenuators are useful. Particularly, a high linearity characteristic is a key requirement in most modern wireless communication systems. In this design, LNA uses 30 dB attenuators to control the gain mode through a power variation of input signals and this attenuator is designed in the pi ( $\pi$ ) type configuration. The output of the attenuator is terminated at 50  $\Omega$ , which shows a minimum distortion characteristic. Therefore, the resistor value is calculated at 50  $\Omega$  terminations

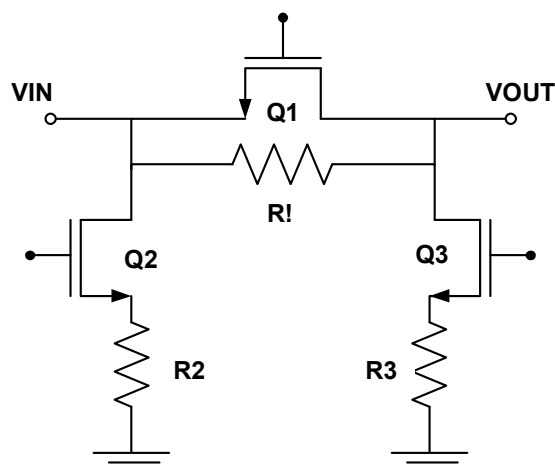


Figure 2. Attenuator with MOS switching

Figure 2 shows a 15 dB attenuator with the MOS switching method. With cascading these, two attenuators obtain 30 dB attenuation. This can be operated through two paths. One is “through path”

and the other is “attenuation path.” When the channel of Q1 is open and those of Q2 and Q3 are OFF, most signals pass through the channel of Q1, called as “Through Pass.” At this condition, the channel resistance and the parasitic capacitance of Q1 can attenuate the signal. For this reason, the size of Q1 is considered to be large. But if the size of Q1 is too large, the parasitic capacitance also increases. Therefore, a careful consideration is needed to study the equivalent circuit of the MOS attenuator circuit that can help design the attenuator as well. When the channel of Q1 is OFF and those of Q2 and Q3 are ON, signals pass through the pi ( $\pi$ ) attenuator. Also, the channel resistance and the parasitic capacitance of Q1, Q2 and Q3 can affect the amount of attenuation and frequency characteristic.

Noisy components in the front of the receiver chain have the most significant impact on the overall noise performance. For this reason, low-noise amplifier (LNA) is placed first on the receiver block [2-5].

## 2-2. Low Noise Amplifier (LNA)

In designing the broadband LNA, there are some difficulties to achieve high gain and low NF characteristics. These two parameters are trade-off. So far there were several topologies for broad band characteristics such as feedback and compensated matching theory. In this work, however, we used the MOS switching filter band selection topology for a broad-band frequency range. The LNA with the MOS switching filter is shown in Figure 3. Figure 4 illustrates the detailed MOS switching filter as a multi-band pass filter. MOS transistors (Q1, Q2) are connected with capacitors which have different values. Resonance frequency is determined by the inductor and capacitor values of the filter, which can be calculated by Equation (1). LNA was designed for the cascade type differential amplifier. The MOS switching filter is connected with inductor loads in parallel and has 2-control-bits. Four-band selection is available by controlling 4-bits of the MOS switching filter [4]. The gate of Q2 in Figure 3 is grounded so that the whole circuit is designed in a single input with differential output.

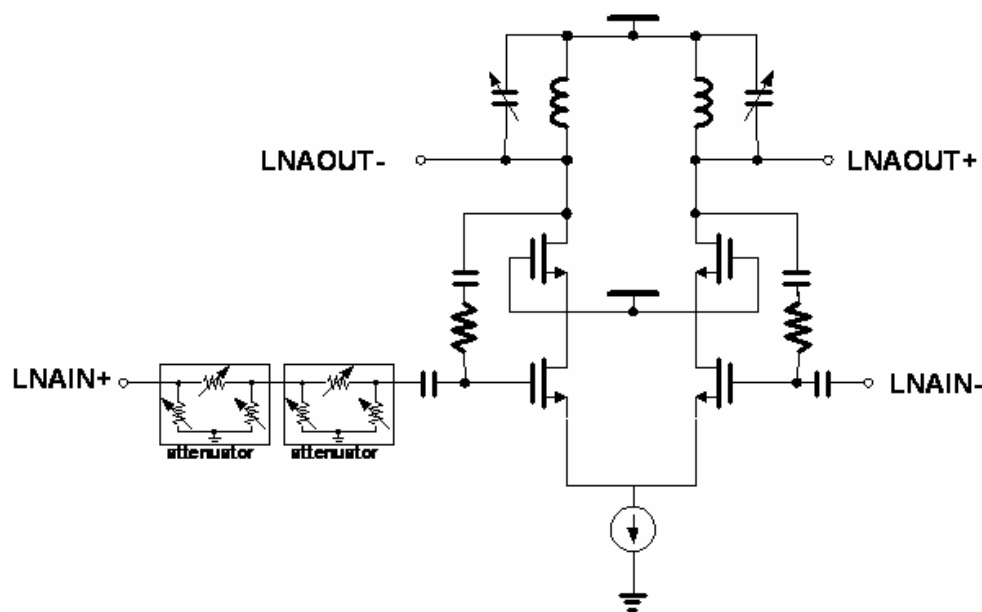


Figure 3. LNA with MOS switching filter.

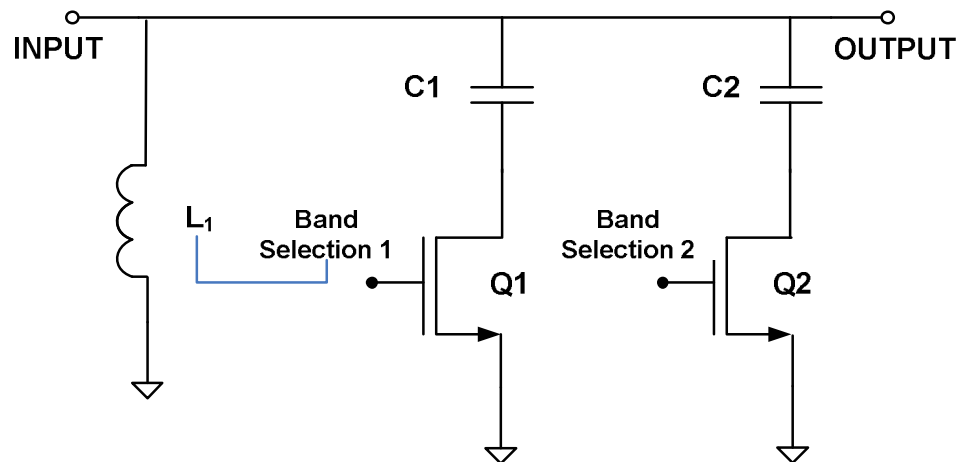


Figure 4. Multi-band pass filter

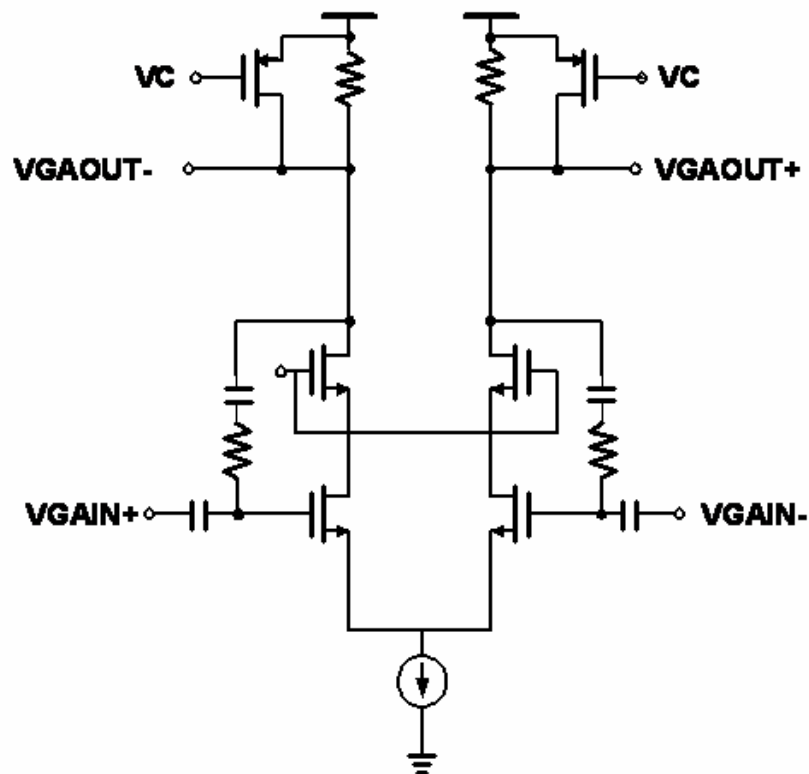


Figure 5. Broadband RF VGA for wide dynamic range.

Q3 and Q4, which are source follower types, take a role of buffer amplifiers. Also the feedback resistor and capacitor made this circuit obtain a good stability and effective noise figure characteristics. The LNA uses load inductors and the MOS switching filter uses capacitors. Each inductor and capacitor have a different value for making different resonant frequencies. Moreover, in order to achieve a flat-gain characteristic (within 3 dB), each frequency band controls the resistor and the size of MOS transistors of the MOS switching filter [6-8].

### 2-3. Radio Frequency Variable Gain Control (RF VGA)

In most communication systems, automatic gain control (AGC) is needed for adjusting the signal amplitude in the receiver (Rx). In this operation, the RF VGA controls the gain of AGC. Generally, AGC is used in heterodyne systems but these days it is needed in the RF system because of common uses of the direct conversion method system structure, meaning that VGA is also needed as RF VGA operated in the RF frequency range [3].

Most conventional CMOS VGAs employ multi-stage architecture to realize a wide dynamic range. But, the result of it can affect the high linearity characteristics when considering the RF VGA location. Therefore, the cascade structure is not effective for linearity and it can be figured out by using Equation (1).

$$\frac{1}{P_{IP3\_Total}} = \frac{1}{P_{IP1\_1}} + \frac{G_1}{P_{IP2\_2}} + \frac{G_1 G_2}{P_{IP3\_3}} \quad (1)$$

In this paper, the high frequency CMOS VGA as a single stage is operated within 950 MHz ~2,150 MHz and is designed with load transistor channel resistance for a wide dynamic range and broad band characteristics [9-11].

The basic design consideration of RF VGA is fully differential. In the differential mode, the common-mode noise can be cancelled, which further can obtain a high the 2<sup>nd</sup> order input intercept point (IIP2) characteristic by canceling the even-order signal input. Figure 5 is the proposed broadband RF VGA circuit for a wide dynamic range. The RF VGA using a differential pair for the fully differential operation is carried out to design a current steering structure in order to achieve a wide dynamic range characteristic. The current steering method uses the feedback of current which flows through the core of the circuit to the steering node by controlling the gate voltage of the steering transistor. The gain-range is decided by the size of steering transistor but this structure cannot be satisfactory for obtaining a wide dynamic range and a high maximum gain at the same time. For this reason, we can obtain RF VGA with a wide dynamic range using CMOS channel resistance. The shunt peaking and feedback techniques are considered for a broad-band frequency range. At this time, the feedback that controls loop gain of the circuit has to be carefully plumbed for the effect on input resistance when it is connected with other blocks. Finally, a multiple-gated transistor (MGTR) technique is also considered for high linearity. The gain range is varied by the differential inductor and the P-MOS channel resistance. The gain can be changed by controlling the resistance load. As shown in Figure 5, the V<sub>c</sub>, gate voltage of P-MOS load, controls the gain range [12-13].

### 3. Experimental Results

The broadband and wide dynamic range LNA/RF VGA is fabricated and characterized using the CMOS 0.18 μm process. The fabricated LNA/RF VGA is shown in Figure 6 and the chip size is 1.4 × 6 mm<sup>2</sup>. The fabricated chip is measured using the SIP (system in package) connection program which provides the condition for effective connectivity before the actual connection between the evaluation board and the test machine. And also, this program can control the DC bias, band selection and modes selection.

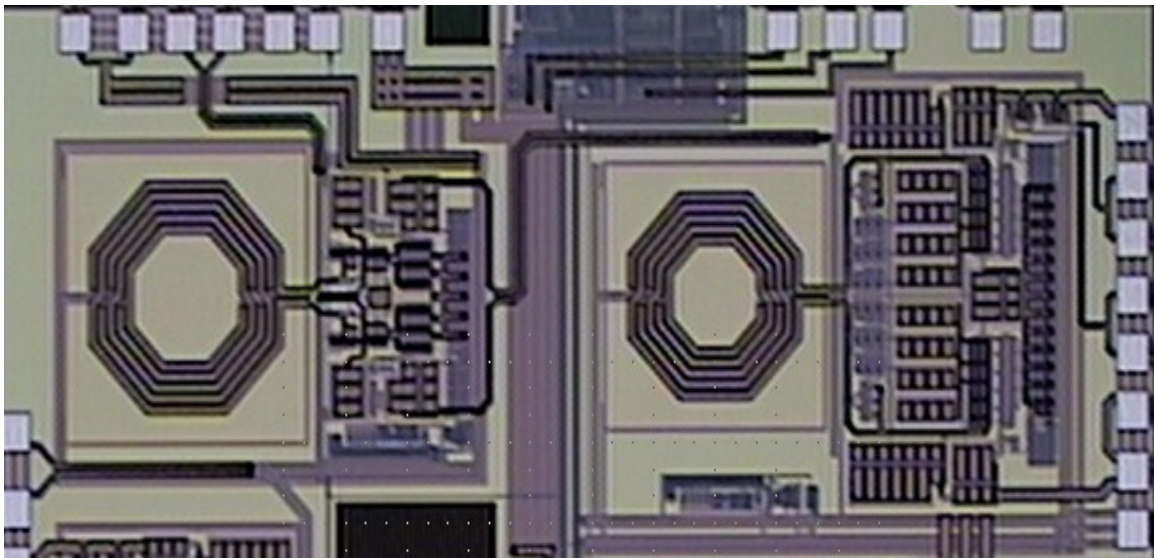


Figure 6. The photograph of fabricated LNA/RF VGA ( $1400 \times 600 \mu\text{m}^2$ ).

The frequency band selection is controlled by the selection bit from 00~11. The peak points through the band selection are 880 MHz, 950 MHz, 1.07 GHz and 13 GHz as shown in Figure 7. It has a gain flatten characteristic lower than 3 dB. Figure 8 shows the measurement result of 3 gain mode by the 30 dB attenuator. Additionally, the gain dynamic range is controlled by RF VGA. The gain mode test of LNA/RF VGA at a low band selection is measured as shown in Figure 9. Also the graphic expression shows the gain modes control being high gain (S21mHG),

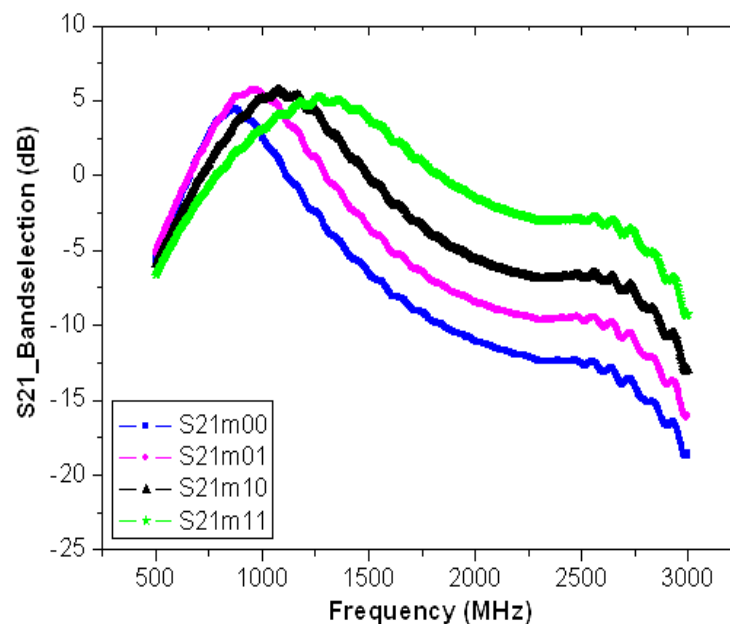


Figure 7. Measurement result of band selection for broadband characteristic.

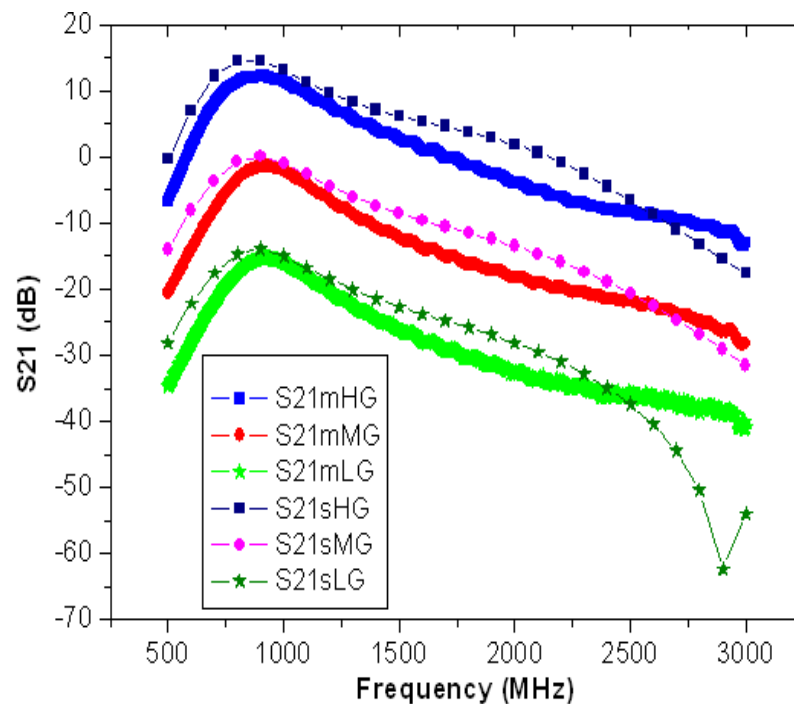


Figure 8. Gain mode test of LNA/RF VGA at low band selection (S21 indicates the simulation results and S21m, the measurement results).

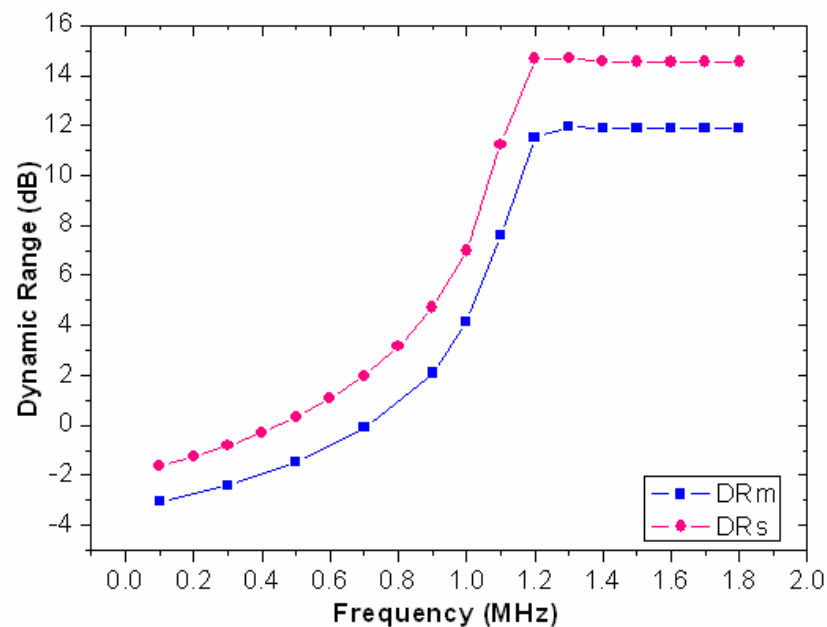


Figure 9. Gain mode test of LNA/RF VGA at low band selection. (DRs indicates the simulation results and DRm, the measurement results).



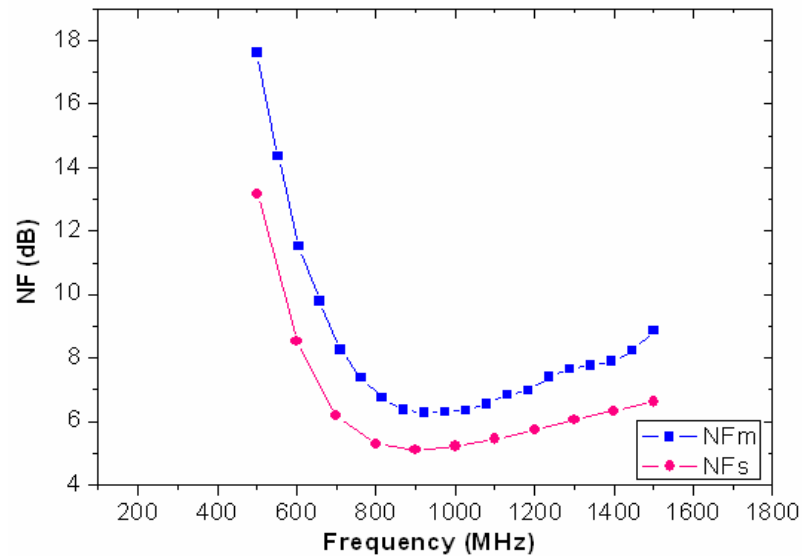


Figure 10. Noise figure at the operation frequency.

Table 1. Summary of measurement results.

| Parameters                  | Unit    | Measurement |
|-----------------------------|---------|-------------|
| Frequency range             | MHz     | 950 ~ 2,150 |
| Power consumption           | mW (mA) | 48.6 (28)   |
| Noise figure(@ High gain)   | dB      | 6.3~7.2     |
| Gain (@ High gain)          | dB      | 23~24       |
| Gain Dynamic range          | dB      | 49.5        |
| IIP3 @ Low band (@Low gain) | dBm     | 15          |

mid gain (S21mMG) and low gain (S21mLG) modes while comparing the simulation results with the similar manner indicating S21sHG, S21sMG and S21sLG. Figure 10 shows the noise figure with a comparison of the simulation result as 7.2 dB at a low band selection. The the 3<sup>rd</sup> order input intercept point (IIP3) is 13.08 dBm at low band and low gain modes [6]. Table 1 shows the summary of the over all measurement performance.



## Conclusion

The broadband and wide dynamic range LNA/RF VGA with the low power consumption has been fabricated by the commercial 0.18 CMOS process. In this work, the MOS switching filter technique is introduced to achieve a broadband characteristic of LNA. The MOS channel resistance was used to get a wide dynamic range RF VGA. The LNA/RF VGA has three gain modes due to the use of an attenuator in the front of LNA. The measurement results show a total current consumption of 28 mA, a gain dynamic range of 50 dB, a noise figure of 7.2 dB at the maximum gain mode, and IIP3 of +15 dBm IIP3 at low gain and low band selection modes has been achieved. This integrated circuit reveals practical significance in the DVB-S2 receiver system.

## Acknowledgements

This research was supported by Nano IP/SoC Promotion Group of the Seoul R&D program (10560) in 2009 and MKE (Ministry of Knowledge Economy), Korea under the ITRC (Information Technology Research Center) support program supervised by the IITA (Institute of Information Technology Assessment) (IITA-2009-C1090-0902-0018). This work also has been supported from the research grant from Kwangwoon University in 2010.

## References:

1. Tsividis Y. (1998), "Operation and modeling of the MOS transistor, McGraw-Hill, Boston.
2. Lawrence E. Larson (1996), "RF and Microwave circuit design for wireless communications", Artech House Publishers.
3. . Fong K. L and Meyer R.G. (2006), "The second generation standard for satellite broad-band services", Proc of the IEE, pp. 210-227.
4. Shin S. C, Lin C. S, Tsai M. D, Lin K. Y (2006), "A low-voltage and variable-gain distributes amplifier for 3.1-10.6 GHz UWB systems", IEEE Microwave Wireless Compon Lett 16, pp. 179-181.
5. Lerstaveesin S., Gupta M., Kang D. and Song B.S. (2008), "A 48-860 MHz CMOS Low-IF Direct Conversion DTV Tuner", IEEE J Solid-State Circuits, Vol. 43, pp. 2013-2024.
6. Kim C.W., Jung M.S. and Lee S.G. (2005), "Ultra-wideband CMOS low noise amplifier", IEE Electronics Lett, Vol. 41, pp. 384-385.
7. Kim C.W., Kang M. S., Tuan P., Kim H. T. and Lee S.G. (2005), "An Ultra-Wideband CMOS Low Noise Amplifier for 3-5 GHz UWB System, IEEE J Solid-State Circuits, Vol. Vol. 40, pp. 544-547.
8. Bevilacqua A., Niknedjad A. M. (2004), "An Ultra-Wideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receiver", 2004 Proc of IEEE International Solid-State Circuits Conference, San Francisco, Calif, USA, pp. 382-533.
9. Razavi B., Aytur T., Yang F.-R., et al. (2005), "A 0.13  $\mu\text{m}$  CMOS UWB Transceiver", in Proceedings of IEEE International Solid-State Circuits Conference, Francisco, Calif, USA, pp. 216-594.
10. Chen W.H., Liu G, Zdravko B. et al. (2008), "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation", IEEE J Solid-State Circuits, Vol. 43, pp.1164-1176.
11. Ming G, Zhang X., Hu X., Hua X. et al. (2008), "A Wide-band front-end for DVB-H tuner

receptions, IEEE International Conference, Solid-State and Integrated Circuit Technology, pp. 1464-1467.

12. Taleje S., HaM.Y. n, Copani T., Bakkaloglu B., Kiaei S. (2008), "A 0.18 um CMOS fully integrated RFDAC and VGA for WCDMA Transmitters", Radio Frequency Integrated Circuits Symposium, pp. 157-160.
13. Duong Q.H., Kim T. J., E -J, Lee S. G. (2006), "An All CMOS 743 MHz Variable Gain Amplifier for UWB Systems, IEEE International Symposium on Circuit and Systems, pp. 678-681.

-----